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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,193	10/28/2003	Joseph P. Dower	Dower 1-1	4280

41119 7590 03/22/2005

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EXAMINER	
PERT, EVAN T	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,193	DOWER ET AL.	
	Examiner	Art Unit	
	Evan Pert	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 5, 6, 7, 9, 12, 13 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Hnilo et al. (US 6,465,898).

Regarding claim 1, the method of the Hnilo et al. reference [abstract] includes two (Fig. 3) alignment marks (400), which are actually formed "in" the "passivation layer 412" on semiconductor chip surface (410).

Regarding claim 2, the method includes selectively processing a portion of the chip using the marks to locate the portion (i.e. wire bonding positioning using the, processing selected as adding material (i.e. adding wire bond materials).

Regarding claim 5, the alignment marks (400) include etched areas in the top surface of "passivation layer 412" (Fig. 4).

Regarding claim 6, the marks are in the shape of crosses (col. 5, lines 11-13, wherein the "features" for fine alignment are "readily recognized as a cross formed by inner segments [of the alignment mark]).

Regarding claim 7, the marks include rectangular portions at ends of the crosses [cover figure] and the number of portions (i.e. 1 or 0) at ends of crosses depend on the quadrant of the chip in which the mark is positioned [col. 4, line 60 to col. 5, line 10].

Regarding claim 9, the semiconductor chip cross section of Fig. 4 shows passivation layer 412 (as a top layer for wire 411, for example), and at least two alignment marks (cover figure) are formed "in" the passivation layer 412, to provide topological features for locating selected areas of the chip [col. 4, line 60 to col. 5, line 10].

Regarding claim 12, the marks 400 include an etched area of passivation 412, wherein the etched area is etched into the "top surface" of the "passivation."

Regarding claim 13, the marks are in the shape of crosses [while not a cross of prior art as stated at col. 2, lines 6-9, the features are arranged such that a "cross" is "readily recognized" col. 5, lines 11-13].

Regarding claim 14, the marks include rectangular portions at ends of the crosses, the number or portions (i.e. 1 or 0) depending on the quadrant in which the mark is located (to distinguish chip corner 303 from chip corner 304, for example).

3. Claims 1, 3, 4, 5, 8, 9, 10, 11, 12 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Thomas et al. (US 5,346,858).

Regarding claim 1, the Thomas et al. reference discloses a method of fabricating a semiconductor chip [abstract], wherein the method includes a top passivation layer (15) with alignment marks (19 of the cover figure) being formed in/on this layer by etching away patterns, shown as triangles in the cover figure.

Regarding claim 3, the alignment marks "comprise metal" because borders of metal 15 define the marks 19.

Regarding claim 4, the chip includes underlying passivation (12), and the alignment marks (19) are formed by depositing material (i.e. material for forming layer 15) over the underlying passivation layer, and then covering with the top passivation layer (i.e. 15 covers 12, and 15 forms alignment markings 19).

Regarding claim 5, the alignment marks (19) comprise etched areas (see col. 2, line 66 to col. 3, line 4) formed in the top surface of the passivation layer (15).

Regarding claim 8, the cover figure shows 8 markings with two in each "corner", a corner being considered one of four quadrants of the chip as applicant did not define how far from center of a polygon one needs to be to be in "a corner").

Regarding claim 9, the Thomas et al. reference shows a chip on the front cover with a top layer passivation (15), and at least two alignment marks (19) formed in/on the layer 15 by etching away patterns in the layer 15 to show the underlying passivation 12, wherein these *alignment marks* 19 *necessarily* "provide topological features for locating selected areas of the chip."

Regarding claim 10, the alignments marks (19) comprise "a metal formed on a top surface of the passivation layer" because the metal borders formed from layer 15 define the alignment marks 19.

Regarding claim 11, the chip includes an additional underlying passivation layer (12), and the alignment marks 19 are formed over the underlying passivation 12 by borders etched in overlying passivation material 15, wherein the passivation 12 is covered by the passivation 15.

Regarding claim 12, the alignment marks 19 are patterns in the top surface of 15, being etched away in the top surface of passivation layer 15.

Regarding claim 15, the cover figure shows at least 4 marks, every quadrant (i.e. corner) having a marking 19.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The documents cited (i.e. US 6,392,300, US 6,278,193, JP 1-241116, and JP 2001-7274) are relevant in that they disclose alignment marks on external passivation features of semiconductor chips.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan Pert whose telephone number is 571-272-1969. The examiner can normally be reached on M-F (7:30AM-3:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EVAN PERT
PRIMARY EXAMINER

ETP
March 16, 2005